In the Claims:

1. (original) A system, comprising:

a transition minimized differential signaling (TMDS) receiver on a first substrate configured for receiving at least one of: digital visual interface (DVI) data, and high definition multi-media (HDMI) data;

at least one transmitter processor on the first substrate and receiving data from the TMDS receiver, the transmitter processor being implemented by one of: a field programmable gate array (FPGA), and application specific integrated circuit (ASIC);

at least one wireless transmitter on the first substrate and receiving data from the transmitter processor for wireless transmission thereof;

at least one wireless receiver configured to receive data from the wireless transmitter;

at least one receiver processor receiving data from the wireless receiver, the receiver processor being implemented by one of: a field programmable gate array (FPGA), and application specific integrated circuit (ASIC); and

a transition minimized differential signaling (TMDS) transmitter configured for receiving data from the receiver processor and outputting at least one of: DVI, and HDMI, input signals to a display.

2. (original) The system of Claim 1, wherein the system does not reduce data to a baseband video signal during processing.

3. (original) The system of Claim 1, wherein at least the transmitter processor includes phase-locked loop circuitry for clock stabilization.

4. (original) The system of Claim 1, wherein at least the transmitter processor includes de-jitter circuitry for input data stabilization.

5. (original) The system of Claim 1, wherein at least the transmitter processor applies forward error correction prior to differential encoding of data.

6. (original) The system of Claim 1, wherein at least the transmitter processor outputs I and Q data to the wireless transmitter.

7. (original) The system of Claim 6, wherein the transmitter processor receives three data TMDS data and 1 TMDS clock streams from the TMDS receiver.

8 -10 (canceled).

11. (currently amended) A digital video transmitter, comprising:

a wireless transmitter;

at least one transmitter processor configured to receive a physical signaling stream representing digital video data and based thereon, without rendering baseband information representing the digital video data, outputting a quadrature signal suitable for processing by [[a]] the wireless transmitter; and

a substrate holding the wireless transmitter and the transmitter processor.

12. (original) The digital video transmitter of Claim 11, wherein the processor is an ASIC.

13. (original) The digital video transmitter of Claim 11, wherein the processor is an FPGA.

14. (canceled).

15. (currently amended) The digital video transmitter of Claim [[14]] 11, wherein the transmitter processor includes phase-locked loop circuitry for clock stabilization.

16. (currently amended) The digital video transmitter of Claim [[14]] 11, wherein at least the transmitter processor includes de-jitter circuitry for input data stabilization.

17. (currently amended) The digital video transmitter of Claim [[14]] 11, wherein at least the transmitter processor applies forward error correction prior to differential encoding of data.

18. (currently amended) The digital video transmitter of Claim [[14]] 11, wherein at least the quadrature signal is I and Q data and the physical signaling stream is 3-data and 1-clock TMDS information, and the digital video transmitter further comprises a TMDS receiver coupled to the processor.

19. (currently amended) A digital video receiver, comprising:

at least one receiver processor configured to receive a demodulated quadrature signal and based thereon, without rendering baseband information representing the digital video data, outputting a physical signaling stream representing digital video data;

a wireless receiver communicating with the receiver processor; and

a substrate holding the wireless receiver and the receiver processor.

20. (original) The digital video receiver of Claim 19, wherein the processor is an ASIC.

21. (original) The digital video receiver of Claim 19, wherein the processor is an FPGA.

22. (canceled).

23. (currently amended) The digital video receiver of Claim [[22]] 19, wherein at least the quadrature signal is I and Q data and the physical signaling stream is 3-data and 1-clock TMDS information, and the digital video receiver further comprises a TMDS receiver coupled to the processor.